Amendments to the Claims

The listing of claims will replace all prior versions, and listings of claims in the application.

1. *(currently amended)* An integrated packet bit error rate tester, comprising:

a substrate;

a packet transmit circuit including a first memory for storing transmit bit error rate test packet data, wherein the packet transmit circuit is coupled to a channel under test;

a packet receive circuit including a second memory for storing received packet compare data and coupled to the channel under test;

an interface for programming the packet transmit circuit and the packet receive circuit;

wherein said packet transmit circuit and said packet receive circuit are deposited on said substrate;

wherein the packet transmit circuit generates an arbitrary packet pattern in response to a command from the interface; and

wherein the packet receive circuit determines a bit error rate of the channel under test.

2. *(original)* The integrated packet bit error rate tester of claim 1, wherein the packet transmit circuit includes a first pseudo-random number generator for generating the arbitrary packet pattern.

3. *(original)* The integrated packet bit error rate tester of claim 2, wherein the packet receive circuit includes a second pseudo-random number generator for generating the same arbitrary packet pattern that is generated by the first pseudo-random number generator.

4. *(previously presented)* The integrated packet bit error rate tester of claim 1, wherein the packet transmit circuit includes a byte counter for counting a number of bytes transmitted during bit error rate testing.

5. *(previously presented)* The integrated packet bit error rate tester of claim 1, wherein the packet transmit circuit includes a packet counter for counting a number of packets transmitted during bit error rate testing.

6. *(original)* The integrated packet bit error rate tester of claim 1, wherein the packet receive circuit includes a bit error counter for counting a number of bit errors detected during bit error rate testing.

7. *(original)* The integrated packet bit error rate tester of claim 1, wherein the packet receive circuit includes a byte error counter for counting a number of bytes with at least one bit in error detected during bit error rate testing.

8. *(original)* The integrated packet bit error rate tester of claim 1, wherein the packet receive circuit includes a packet error counter for counting a number of packets with at least one byte in error detected during bit error rate testing.

9. *(previously presented)* The integrated packet bit error rate tester of claim 1, wherein the second memory captures the received packet compare data only after a pre-programmed pattern is detected.

10. *(original)* The integrated packet bit error rate tester of claim 9, wherein the pre-programmed pattern includes a fixed pattern.

11. *(original)* The integrated packet bit error rate tester of claim 9, wherein the pre-programmed pattern includes a programmable pattern.

12. *(previously presented)* The integrated packet bit error rate tester of claim 9, wherein the pre-programmed pattern includes a cyclic redundancy check pattern.

13. *(previously presented)* The integrated packet bit error rate tester of claim 1, wherein the arbitrary packet pattern is received from an external random access memory.

14. *(previously presented)* The integrated packet bit error rate tester of claim 1, wherein the arbitrary packet pattern can be loaded into a random access memory for bit error rate testing.

15. *(previously presented)* The integrated packet bit error rate tester of claim 1, wherein the second memory captures the received packet compare data only after a pre-programmed pattern is lost.

16. *(previously presented)* The integrated packet bit error rate tester of claim 1, wherein the second memory captures the received packet compare data only after an error is detected.

17. *(previously presented)* The integrated packet bit error rate tester of claim 1, wherein the second memory captures the received packet compare data continuously.

18. *(previously presented)* The integrated packet bit error rate tester of claim 1, further including a finite state machine for controlling capture of the received packet compare data.

19. *(original)* The integrated packet bit error rate tester of claim 1, wherein the packet receive circuit includes a byte counter for counting a total number of bytes received.

20. *(original)* The integrated packet bit error rate tester of claim 1, wherein the packet receive circuit includes a packet counter for counting a total number of packets received.

21. *(original)* The integrated packet bit error rate tester of claim 1, wherein the packet transmit circuit includes a byte counter for counting a total number of bytes transmitted.

22. *(original)* The integrated packet bit error rate tester of claim 1, wherein the packet transmit circuit includes a packet counter for counting a total number of packets transmitted.

23. *(previously presented)* The integrated packet bit error rate tester of claim 1, wherein the arbitrary packet pattern is a ten gigahertz serializer / deserializer packet.

24. *(currently amended)* An integrated packet bit error rate tester, comprising:

a substrate;

a packet transmit circuit including a first memory for storing transmit bit error rate test packet data, wherein the packet transmit circuit is coupled to a channel under test;

a packet receive circuit including a second memory for capturing received packet compare data from the channel under test;

an interface for programming the packet transmit circuit and the packet receive circuit;

wherein said packet transmit circuit and said packet receive circuit are deposited on said substrate;

wherein the packet transmit circuit generates an arbitrary serializer / deserializer (SERDES) packet pattern in response to a command from the interface; and

wherein the packet receive circuit determines a bit error rate of the channel under test based on the transmit packet data compared to the receive packet data.

25. *(original)* The integrated packet bit error rate tester of claim 24, wherein the packet receive circuit includes a byte counter for counting a total number of bytes received.

26. *(original)* The integrated packet bit error rate tester of claim 24, wherein the packet receive circuit includes a packet counter for counting a total number of packets received.

27. *(original)* The integrated packet bit error rate tester of claim 24, wherein the packet transmit circuit includes a byte counter for counting a total number of bytes transmitted.

28. *(original)* The integrated packet bit error rate tester of claim 24, wherein the packet transmit circuit includes a packet counter for counting a total number of packets transmitted.

29. *(original)* The integrated packet bit error rate tester of claim 24, wherein the packet transmit circuit includes a first pseudo-random number generator for generating the arbitrary SERDES packet pattern.

30. *(original)* The integrated packet bit error rate tester of claim 29, wherein the packet receive circuit includes a second pseudo-random number generator for generating the same arbitrary SERDES packet pattern that is generated by the first pseudo-random number generator.

31. *(original)* The integrated packet bit error rate tester of claim 29, wherein the second memory captures the received packet data only after a pre-programmed pattern is detected.

32. *(original)* The integrated packet bit error rate tester of claim 31, wherein the pre-programmed pattern includes a fixed pattern.

33. *(original)* The integrated packet bit error rate tester of claim 31, wherein the pre-programmed pattern includes a programmable pattern.

34. *(previously presented)* The integrated packet bit error rate tester of claim 31, wherein the pre-programmed pattern includes a cyclic redundancy check pattern.

35. *(original)* The integrated packet bit error rate tester of claim 24, wherein the second memory captures the received packet data only after a pre-programmed pattern is lost.

36. *(original)* The integrated packet bit error rate tester of claim 24, wherein the second memory captures the received packet data only after an error is detected.

37. *(previously presented)* The integrated packet bit error rate tester of claim 24, wherein the second memory captures the received packet data continuously.

38-40. *(canceled).*

41. *(currently amended)* A method of testing a bit error rate of a channel coupled to a transmitter memory deposited on a substrate and to a receiver deposited on the substrate, comprising:

generating a test packet including an arbitrary marker pattern;

loading the test packet into the transmitter memory;

transmitting the test packet from the transmitter memory over the channel;

capturing a received test packet from the channel; and

determining the bit error rate of the channel based on the received test packet.

42. *(previously presented)* The method of claim 41, further including generating an arbitrary ten gigahertz serializer / deserializer (10G SERDES) packet pattern.

43. *(previously presented)* The method of claim 42, further including generating the arbitrary 10G SERDES packet pattern using a first pseudo-random number generator.

44. *(previously presented)* The method of claim 42, further including programming the arbitrary 10G SERDES packet pattern through a management data input/output interface.

45. *(previously presented)* The method of claim 42, further including generating the same arbitrary 10G SERDES packet pattern using a second pseudo-random number generator as the 10G SERDES packet pattern generated by the first pseudo-random number generator.

46. *(original)* The method of claim 41, further including counting a number of bytes received during the bit error rate testing.

47. *(original)* The method of claim 41, further including counting a number of packets received during the bit error rate testing.

48. *(original)* The method of claim 41, further including counting a number of bit errors detected during the bit error rate testing.

49. *(original)* The method of claim 41, further including counting a number of bytes with errors detected during the bit error rate testing.

50. *(original)* The method of claim 41, further including counting a number of packets with a byte in error detected during the bit error rate testing.

51. *(original)* The method of claim 41, further including determining a bit error rate of the channel under test.

52. *(original)* The method of claim 41, further including counting a number of packets transmitted over the channel.

53. *(original)* The method of claim 41, further including counting a number of number of bytes transmitted over the channel.